IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled)

2. (Previously presented) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating a beeline distance on a substrate from each of said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum beeline distance to said scan data input terminal of said second memory element with said scan data input terminal of said second memory element.

3-4. (Cancelled)

5. (Previously presented) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum wire length with said scan data input terminal of said second memory element.

6-7. (Cancelled)

8. (Previously presented) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element; and

connecting one of aid output terminals having minimum fan-out with said scan data input terminal of said second memory element.

9-11. (Cancelled)

12. (Previously presented) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element; and

connecting one of said output terminals of said first memory element having a minimum load capacitance with said scan data input terminal of said second memory element.

13-20. (Cancelled)